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EXAMINER	
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ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,025	CHAPMAN, JOHN T.	
	Examiner	Art Unit	
	Venkatesh Haliyur	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/11/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Dworkin et al [US Pub: 2003/0058893].

Regarding claim 1, Dworkin et al in the invention of "Synchronization of Multiple Cable Modem Termination Systems" disclosed a synchronization circuit **(synchronization circuit, item 223 of Fig 2, para 0048)**, comprising: a local timestamp counter **(TGC counter)** configured to generate a local timestamp value **(current time value)**; and a processing circuit **(processor, item 222 of Fig 2)** to receive synchronization pulses and a predicted master timestamp value **(future time value)** for a next synchronization pulse, the processing circuit to identify the local timestamp value at the next received synchronization pulse and synchronize the local timestamp counter

according to the identified local timestamp value and the predicted master timestamp value **(para 0010)**; the processing circuit to receive an error message indicating that the predicted master timestamp value is not equal to an actual master timestamp value for the next synchronization pulse **(generate calibration pulse is issued for time differentials)**; and the processing circuit to predict a new master timestamp value in response to the error message **(para 0010, lines 11-29).**

Regarding claims 2,5, Dworkin et al disclosed that the processing circuit **(item 104 of Fig 2)** is located in a Cable Modem Termination System and receives the predicted master timestamp value from another CMTS **(item 104A of Fig 1)** and the synchronizing circuitry comprises processing circuitry to send the new predicted master timestamp value **(FTSV)** to the another CMTS **(item 104B of Fig 1) (Fig 1, para 0048).**

Regarding claims 3-4, Dworkin et al disclosed that the processing circuit receives the predicted master timestamp value asynchronously in Internet Protocol **(IP)** packets received over an IP connection **(para 0038)** and including a holding register configured to store the received predicted master timestamp value **(para 0010, lines 31-41).**

Regarding claims 6-7, Dworkin et al disclosed that the synchronization pulse has a rate of somewhere between 8 Kilo Hertz and 1 Hertz **(single or specific calibration pulse generator, para 0039)** and the processing circuit identifies an error condition **(compare registers for errors)** according to a number of times the local timestamp counter is synchronized with master received timestamp values **(para 0092,0093)**.

Regarding claim 8, Dworkin et al disclosed multiple line cards in a same Cable Modem Termination System chassis **(back plane, item 100 of Fig 1)** that each have

local timestamp counters **(TGC counters)** that are adjusted according to the received predicted master timestamp value **(future timestamp value, FTSV, para 0010)** and local timestamp values at the next received synchronization pulse **(para 0041)**.

Regarding claim 9, Dworkin et al disclosed a first CMTS **(item 104B of Fig 1)** including one or more line cards that are used for downstream channels **(para 0039)** and a second CMTS including one or more line cards that are used for upstream channels **(para 0040)**, cable modems receiving data on the downstream channels of the first CMTS and sending data on the upstream channels of the second CMTS **(para 0041)**.

Regarding claim 10, Dworkin et al disclosed a synchronization system **(Figs 1-3)**, comprising: a master synchronization circuit **(Fig 2)** configured to: identify a first master timestamp value associated with a first synchronization pulse and a second master timestamp value associated with a second synchronization pulse **(internal pulses generated by each CMTS device, para 0071)**, determine a difference between the first and second master timestamp values **(compare circuit, item 306 of Fig 3, para 0072)** and an amount of time occurring between the first and second synchronization pulses **(repeat cycle)**; predict the occurrence of a future synchronization pulse at a time equal to the amount of time multiplied by a predetermined amount **(generate a periodic internal pulse rate, para 0073)**; calculate a future master timestamp value **(TGC counter values)** that corresponds to the future synchronization pulse **(FTSV)** by adding the second master timestamp value and the difference multiplied by the predetermined amount **(para 0083)**; forward the calculated future master timestamp value to a slave

synchronization circuit for synchronizing at the future synchronization pulse **(para 0084-0087).**

Regarding claims 11-12, Dworkin et al disclosed that the master synchronization circuit is further configured to: identify an actual master timestamp value **(TGC counter current value)** corresponding to the future synchronization pulse when the future synchronization pulse occurs **(para 0085)**; determine whether a difference between the actual master timestamp value and the future master timestamp value is within a predetermined range; and send an error message to the slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range **(para 0086)** and the slave synchronization circuit is configured to calculate and forward new future master timestamp values in response to receiving the error message **(Fig 4, para 0087-0090).**

Regarding claims 13-15, Dworkin et al disclosed that a first Cable Modem Termination Systems (CMTS) having a first chassis **(back plane)** containing the master synchronization circuit and a second CMTS having a second separate chassis containing the slave synchronization circuit **(for each of the master and slave CMTS, items 104A, 104B of Fig 1, para 0041)** and that multiple lines cards in at least one of the first and second CMTS that includes multiple slave circuits each synchronized with the future master timestamp value at the future synchronization pulse when the difference between the actual master timestamp value and the future master timestamp value is within the predetermined range at the later occurring synchronization pulse **(para 0048)** and the slave synchronization circuit adjusts the received calculated future

master timestamp value according to an amount of delay associated with receiving the synchronization pulses **(para 0052).**

Regarding claim 16, Dworkin et al disclosed a method for synchronizing circuitry **(Figs 1-2)**, comprising: receiving an extrapolated master timestamp value **(new value)** for an upcoming time reference over an asynchronous connection **(received over IP network, para 0043)**; generating a local timestamp value **(current value)**; comparing the local timestamp value at the upcoming time reference with the extrapolated master timestamp value **(FTSV, para 0010)**; and synchronizing the local timestamp value according to the comparison **(para 0048,0057).**

Regarding claim 17, Dworkin et al disclosed a method identifying a period between synchronization pulses; extrapolating a time for a future synchronization pulse by adding one of the synchronization pulses to the period multiplied by a predetermined amount **(TGC base value, para 0074-0078)**; and extrapolating the master timestamp value by adding a master timestamp value for the one of the synchronization pulses **(para 0010)** and the predetermined amount multiplied by a difference between two previous master timestamp values **(para 0079-0083, Figs 4-5)**.

Regarding claim 18, Dworkin et al disclosed a method including receiving the extrapolated master timestamp value from a first cable modem termination system (CMTS) and using the extrapolated master timestamp value to synchronize a timing circuit in a second CMTS **(para 0082).**

Regarding claim 19, Dworkin et al disclosed a method according to claim 16 including: synchronizing the timing circuitry in a first Cable Modem Termination System

(CMTS) with the timing circuitry in a second CMTS; using the first CMTS to send data to cable modems **(items 106 and 108 of Fig 1)**; and using the second CMTS to receive data from the same cable modems **(para 0043).**

Regarding claim 20, Dworkin et al disclosed a method according to claim 16 further including-receiving an error message indicating that the predicted master timestamp value is not equal to an actual master timestamp value for the next synchronization pulse **(time differential, para 0076)**; predicting a new master timestamp value in response to the error message **(para 0078)**; and sending the predicted new master timestamp value to a generation source of a message including the received extrapolated master timestamp value **(new value, para 0079-0082).**

Regarding claims 21-22, Dworkin et al disclosed the predicted master timestamp value is equal to a sum of an actual master timestamp value for a previous synchronization pulse and a predetermined amount multiplied by a difference between two previous actual master timestamp values **(para 0083)** and the predefined amount is equal to a quotient of a difference in time between the previous synchronization pulse and the next synchronization pulse divided by a period between synchronization pulses that corresponds to the two previous actual master timestamp values **(offset values, para 0084-0085).**

Conclusion

5. Any inquiry concerning this communication or earlier communications should be directed to the attention to Venkatesh Haliyur whose phone number is 571-272-8616. The examiner can normally be reached on Monday-Friday from 9:00AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached @ (571)-272-7493. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (571)-272-2600 or fax to 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Venkatesh Haliyur

Patent Examiner

04|27|07

WING CHAN
SUPERVISORY PATENT EXAMINER